## REMARKS

The Office Action mailed August 29, 2001, has been received and reviewed. Claims 1 through 29 are currently pending in the application. Claims 21 through 29 have been withdrawn from consideration as being drawn to a non-elected invention. Claims 1 through 20 stand rejected. Applicants have amended claim 2, and respectfully request reconsideration of the application as amended herein.

**Objection to Specification**

The title of the invention was objected to as being "not descriptive". The title has been amended as set forth above in accordance with the Examiner's requirement.

**35 U.S.C. § 102 Anticipation Rejections**

Claims 1 through 20 stand rejected under 35 U.S.C. §§ 102(a) and 102(e) over various United States Patents. A claim is anticipated only if each and every element as set forth in the claim is found, either expressly or inherently described, in a single prior art reference. *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). The identical invention must be shown in as complete detail as is contained in the claim. *Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Applicants respectfully traverse each of the recited anticipation rejections because the cited references fail to describe each and every element of each of the claims of the present invention.

Anticipation Rejection Based on U.S. Patent No. 5,894,107 to Lee et al.

Claims 1 through 20 stand rejected under 35 U.S.C. § 102(a) as being anticipated by Lee et al. (U.S. Patent No. 5,894,107). Applicants respectfully traverse this rejection, as hereinafter set forth.

Lee et al. describes the formation of an encapsulated chip-scale package including two lead frames, wherein a second lead frame includes a plurality of rows of external connection

means 34. An upper surface of the external connection means 34 is exposed outside of the material encapsulating the lead frames. More specifically, "the upper surfaces of the external connection means 34 are exposed toward the outside for electrical connection to the external interconnections." *See, Lee et al.* at col. 5, lines 21-24. "[S]older balls 16 are attached to the exposed upper surfaces of the external connection means 34 of the second lead frame." *See, Lee et al.* at col. 5, lines 39-43 (emphasis added). Thus, Lee et al. describes the formation of a chip-scale package wherein solder balls are attached on an outer surface of the encapsulated portion of the chip-scale package.

Independent claim 1 is directed to a chip-scale package and recites as an element of the claim "at least one carrier bond" and "an encapsulant material encapsulating...a portion of the at least one carrier bond." Similarly, independent claim 2 recites "a plurality of conductive carrier bonds" and "an encapsulating material disposed about...a portion of each carrier bond of said plurality of conductive carrier bonds." Lee et al. fails to anticipate these claims because Lee et al. fails to expressly, or inherently, describe an encapsulating material encapsulating, or disposed about, a carrier bond as claimed in claims 1 and 2. *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987). Rather, Lee et al. describes a solder ball, which is compared by the Office to the carrier bonds of the present invention, attached to the outer surface of an external connection means that extends to the outer surface of an encapsulating material about a chip-scale package. The encapsulating material described by Lee et al. does not encapsulate a portion of the solder balls, and is not disposed about a portion of the solder balls. Thus, Lee et al. fails to anticipate both independent claims 1 and 2.

Claims 3 through 20 depend from claim 2 and are therefore allowable over the anticipation rejection based upon Lee et al. because Lee et al. fails to describe a structure identical to that claimed by claim 2, and in as complete detail as claim 2. *See, Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Anticipation Rejection Based on U.S. Patent No. 6,181,010 to Nozawa

Claims 1 through 20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Nozawa (U.S. Patent No. 6,181,010). Applicants respectfully traverse this rejection, as hereinafter set forth.

Nozawa describes the formation of a semiconductor device including an interconnect layer 120 in contact with electrodes 104 of a semiconductor chip 100 and a conducting layer 122 contacting the interconnect layer 120. An underlying metal layer 124 contacts the conducting layer 122 for supporting bumps 200 or solder balls. In various embodiments of the Nozawa invention, a resin layer 126 encompasses portions of the semiconductor device, but never the underlying metal layer 124 or bumps 200.

Nozawa fails to anticipate claims 1 and 2 of the present invention for at least two reasons. First, the bumps 200 of Nozawa are construed by the Office as the "at least one carrier bond" of claim 1, or the "plurality of conductive carrier bonds" recited in claim 2. In either case, Nozawa fails to anticipate the claims because the resin layer 126, or alleged encapsulating material, is not disposed about, and does not encapsulate, any portion of the bumps 200. Claims 1 and 2 of the present invention, however, specifically claim that an encapsulating material either encapsulates a portion of the at least one carrier bond (Claim 1) or is disposed about at least a portion of each carrier bond (Claim 2). Nowhere does Nozawa describe such a feature, therefore, the anticipation rejection of claims 1 and 2 should be withdrawn. *See*, *Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

In addition, Nozawa fails to describe the "at least one conductive bond connecting the at least one conductive trace to the at least one bond pad on the active surface of said semiconductor die" as recited in claim 1. Hypothetically assuming that the electrode 104 of Nozawa is the equivalent of a bond pad claimed by claim 1, and that the interconnect layer 120 is the equivalent of a conductive trace as recited by claim 1, Nozawa does not describe a conductive bond connecting those two elements. Thus, Nozawa fails to describe all of the elements of claim

1, precluding an anticipation rejection. *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

For the same reasons, Nozawa fails to describe the plurality of conductive bond members connecting conductive traces to bond pads recited in claim 2. Therefore, claim 2 is not anticipated.

Claims 3 through 20 depend from independent claim 2, which is allowable over Nozawa. Because independent claim 2 is allowable, so too are claims 3 through 20 because Nozawa fails to describe all of the elements of the independent claim from which the dependent claims depend.

Furthermore, at least claims 8 through 12 are independently allowable over Nozawa because Nozawa does not describe a conductive bond member, let alone the different types of conductive bond members recited in claims 8 through 12.

Anticipation Rejection Based on U.S. Patent No. 6,144,102 to Amagai

Claims 1 through 20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Amagai (U.S. Patent No. 6,144,102). Applicants respectfully traverse this rejection, as hereinafter set forth.

Amagai describes a semiconductor device package comprising an insulating substrate 3 having conductor leads 7 formed thereon, with through-holes 6 formed through insulating substrate 3 to expose circular regions 7*b* of conductor leads 7. In the finished semiconductor device, solder fills the through-holes 6, thereby forming connections for the placement of solder bumps 11 over the filled through-holes 6. *See, Amagai* at col. 5, lines 50-55. Furthermore, portions of conductor leads 7 are connected to electrode pads 2 of a semiconductor chip 1 by conductor wires 9. The semiconductor chip 1 is connected to the insulating substrate 3 and conductor leads by adhesive layer 8. A resin 10 is used to cover the conductor wires 9 and openings to a portion of the leads 7 and electrode pads. *See, Amagai* at col. 5, lines 38-40.

Claim 1 of the present invention specifically recites:

> an encapsulant material encapsulating said semiconductor die, the at least one conductive trace, the at least one conductive bond, and a portion of the at least one carrier bond, the at least one carrier bond having another portion extending beyond said encapsulant material.

Amagai does not describe an encapsulant material as recited in claim 1. If the resin 10 material of Amagai is the alleged encapsulant material, the resin 10 fails to encapsulate a portion of the bumps 11 that are purported to be the carrier bonds. If the insulating substrate 3 of Amagai is the alleged encapsulant material, it fails to encapsulate the conductor wires 9 that are allegedly the at least one conductive bond. Either way, Amagai fails to describe an identical invention to claim 1 in as complete detail as is contained in the claim. Amagai fails to anticipate claim 1. *See, Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989).

Similarly, Amagai fails to anticipate independent claim 2 which recites "an encapsulating material disposed about at least...said plurality of conductive bond members and a portion of each carrier bond of said plurality of conductive carrier bonds." Amagai does not describe any structure that anticipates the encapsulating material claimed in claim 2 because no single Amagai element is disposed about both the conductor wires 9 and bumps 11. The failure of Amagai to describe the encapsulating material of claim 2 precludes the present anticipation rejection. *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claims 3 through 20, which depend from claim 2, are also allowable over the anticipation rejection based on Amagai because the elements of claim 2 are included in claims 3 through 20 by dependency. Amagai's failure to describe all of the elements of claim 2 precludes the anticipation rejection of claims 3 through 20.

Anticipation Rejection Based on U.S. Patent No. 6,232,666 to Corisis et al.

Claims 1 through 20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Corisis et al. (U.S. Patent No. 6,232,666). Applicants respectfully traverse this rejection, as hereinafter set forth.

Corisis et al. describes an interconnect for BGA packages comprising a plurality of polymer substrates 32 having a plurality of patterns of conductors 36 formed thereon. The polymer substrates 32, with conductors 36, are attached to a die passivation layer 64 on a face of a semiconductor die 34 by adhesive 62. A metal bump 60 connects conductors 36 to bond pads 46 of die 34. Ball contacts 56 are formed in ball openings 58 of the polymer substrates 32.

In an alternate embodiment, Corisis et al. describes the formation of reflowed solder bumps 78RF for filling a bonding via to physically and electrically bond the conductors 36 to bond pads 46A of a semiconductor die 34B. *See, Corisis et al.* at col. 7, lines 6-10. An encapsulant 76 may be formed over the reflowed solder bumps 78RF.

Corisis et al. fails to anticipate claims 1 and 2 of the present invention because Corisis et al. fail to identically disclose the encapsulant material of claim 1 and the encapsulating material of claim 2. *See, Richardson v. Suzuki Motor Co.*, 9 USPQ2d 1913, 1920 (Fed. Cir. 1989). Claim 1 specifically recites that the encapsulant material encapsulates a portion of the at least one carrier bond. No such encapsulant material is disclosed by Corisis et al. Similarly, claim 2 specifically recites that an encapsulating material is disposed about a portion of each carrier bond. Corisis et al. do not disclose any encapsulating material disposed about a portion of the ball contacts 56 which are allegedly the same as the carrier bonds recited in claim 2. The failure of Corisis et al. to disclose an encapsulant (Claim1) or an encapsulating material (Claim 2) as claimed by the present invention, precludes the current anticipation rejection under 35 U.S.C. § 102(e). *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claims 3 through 20, which depend from claim 2, are also allowable over Corisis et al. because each of the dependent claims 3 through 20 inherit the elements of claim 2 that are not anticipated by Corisis et al.

Anticipation Rejection Based on U.S. Patent No. 6,147,413 to Farnworth

Claims 1 through 20 stand rejected under 35 U.S.C. § 102(e) as being anticipated by Farnworth (U.S. Patent No. 6,147,413). Applicants respectfully traverse this rejection, as hereinafter set forth.

Farnworth describes a semiconductor device and the formation of conductive repattern traces 1016 over bond pads 1002 of the semiconductor device. The conductive repattern traces 1016 are allegedly equivalent to the conductive traces as claimed in claims 1 and 2 of the present invention. Bond pads 1002 are allegedly equivalent to the bond pads on the active surface of the semiconductor dies claimed by the present invention. However, Farnworth fails to describe a conductive bond joining the conductive repattern traces 1016 to the bond pads 1002. Rather, the perpattern traces 1016 of Farnworth are in direct contact with the bond pads 1002.

Claim 1 of the present invention includes "at least one conductive bond connecting the at least one conductive trace to the at least one bond pad on the active surface of said semiconductor die," and claim 2 includes "a plurality of conductive bond members, at least one conductive bond member...connecting each conductive trace...to at least one bond pad." Farnworth does not disclose such structures. The failure of Farnworth to disclose conductive bond members for connecting conductive traces and bond pads precludes the present anticipation rejection. *See, Verdegaal Brothers v. Union Oil Co. of California*, 2 USPQ2d 1051, 1053 (Fed. Cir. 1987).

Claims 3 through 20 are also allowable because they depend from independent claim 2 which is allowable. Farnworth's failure to describe the conductive bond members of claim 2 carries over to claims 3 through 20, which are therefore allowable.

## ENTRY OF AMENDMENTS

The amendments to claim 2 should be entered by the Examiner because the amendments are supported by the as-filed specification and drawings and do not add any new matter to the application.

## CONCLUSION

Claims 1 through 20 are believed to be in condition for allowance, and an early notice thereof is respectfully solicited. Should the Examiner determine that additional issues remain which might be resolved by a telephone conference, he is respectfully invited to contact Applicants' undersigned attorney.

Respectfully Submitted,

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DRJ/ps:dh
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Enclosure: Version With Markings to Show Changes Made

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## VERSION WITH MARKINGS TO SHOW CHANGES MADE

2. (Twice Amended) A chip-scale package comprising:

a semiconductor die having an active surface having a plurality of bond pads thereon;

a dielectric element having an upper surface and a lower surface, the lower surface of said dielectric element attached to a portion of the active surface of said semiconductor die;

a plurality of conductive traces, each trace of the plurality of conductive traces having an upper surface and a lower surface, the lower surface of each trace of said plurality of conductive traces attached to a portion of the upper surface of said dielectric element for connecting each conductive trace of said plurality of conductive traces to the active surface of said semiconductor die;

a plurality of conductive bond members, at least one conductive bond member of the plurality of conductive bond members connecting each conductive trace of said plurality of conductive traces to at least one bond pad of the plurality of bond pads on the active surface of said semiconductor die;

a plurality of conductive carrier bonds, at least one carrier bond of the plurality of conductive carrier bonds disposed on the upper surface of each conductive trace of said plurality of conductive traces; and

an encapsulating material disposed about at least portions of said semiconductor die, said dielectric element, said plurality of conductive traces, said plurality of conductive bond members and a portion of each carrier bond of said plurality of <u>conductive</u> carrier bonds.